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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/802,914 | FUNAHASHI ET AL. | |
| | Examiner | Art Unit | |
| | JARED I. RUTZ | 2187 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *9-11,16-18 and 24-31* is/are pending in the application.

4a) Of the above claim(s) *29-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-11, 16-18, and 24-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 9-11, 16-18, and 24-31, as amended on 1/28/2008, are pending in the instant application. Applicant's arguments submitted 1/28/2008 have been carefully and fully considered, but are not found persuasive. The new grounds of rejection presented in this Office action have been necessitated by amendment. Accordingly, this Office action is made **FINAL**.

### *Election/Restrictions*

2. Newly submitted claims 29-31 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:
The inventions are distinct, each from the other because of the following reasons:

3. Invention I, consisting of claims 9-11, 16-19, and 24-28, is directed to apparatuses for sharing data and a method of sharing data in an apparatus including a first endian type and second endian type processor accessing shared memory, and is classified in class 711.

4. Invention II, consisting of claims 29-31, is directed to a method and apparatus which performs preprocessing to prepare a program to be compiled for a first endian type or second endian type processor, and is classified in class 717.

5. Inventions I and II are directed to related products/processes. The related inventions are distinct if: (1) the inventions as claimed are either not capable of use together or can have a materially different design, mode of operation, function, or effect; (2) the inventions do not overlap in scope, i.e., are mutually exclusive; and (3) the

inventions as claimed are not obvious variants. See MPEP § 806.05(j). In the instant case, the inventions as claimed have a materially mode of operation and effect, as invention I is an apparatus/method which executes programs on processors of different endian types, and invention II prepares written code to be compiled. Furthermore, the inventions as claimed do not encompass overlapping subject matter and there is nothing of record to show them to be obvious variants.

6. Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and examination burden if restriction were not required because one or more of the following reasons apply:

(a) the inventions have acquired a separate status in the art in view of their different classification;

(b) the inventions have acquired a separate status in the art due to their recognized divergent subject matter;

(c) the inventions require a different field of search (for example, searching different classes/subclasses or electronic resources, or employing different search queries);

(d) the prior art applicable to one invention would not likely be applicable to another invention;

(e) the inventions are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 29-31 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

7. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

### *Claim Rejections - 35 USC § 112*

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. **Claim 28** is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

10. **Claim 28** recites the limitations "*a second address bus which is logically connected to said second-endian processor*" and "*a second data bus logically connected to said second-endian processor, said second data bus being logically connected to the first data bus in a first-endian order*". There is insufficient written description support in the specification as originally filed, as there is no mention of a second data bus, a second address bus, or that a second data bus is connected to a first data bus in a first endian order.

### *Claim Rejections - 35 USC § 103*

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. **Claims 9-11, 16-19, and 24-28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lasserre et al. (US 6,760,829) in view of Sartorius et al. (US 5,848,436).

13. **Claim 9** is taught by Lasserre as:

a. *A data sharing apparatus comprising: a data bus having a data width*. Column 8 lines 63-65 show DSP 400 sharing a memory location 410 with a CPU 402, with the DSP 400 and CPU 402 having different endianness. Column 9 4-17 shows that the data bus between the processors and memory is 32 bits.

b. *A memory*. Figure 4 shows a memory storing memory location 410.

c. *A first-endian processor logically connected to said memory in a first-endian byte order via said data bus*. CPU 402.

d. *A second-endian processor logically connected to said memory in the first-endian byte order via said data bus*. DSP 400. Figure 4, as discussed in column 9 lines 12-17, shows that each of the processors are connected to the data bus such that inputs [7:0] of the two processors and the memory are connected to the same lines of the data bus.

e. *And an address conversion unit operable to invert selected address bits and output the adjusted address*. Column 10 line 59 through column 11 line 4 shows that memory controller circuitry 706 inverts the least significant address bits to reverse the address ascension in order to agree with the endianism of the selected memory region. Figure 7 shows adjusted physical address 716 is output by address adjust circuitry 706.

f. *Wherein said memory stores structure data to be accessed by said first-endian processor and said second-endian processor*. Column 9 lines 22-25

shows that a 16 bit value can be written to location 2 of 32 bit memory word 410 of figure 4.

g. *Said first-endian processor executes a first program that defines the structure data*. Column 9 lines 22-25 shows that when a processor in little-endian mode, CPU 402, writes a 16 bit value to location 2 of memory word 410, it will overwrite 0xDDCC, corresponding to lines [31:16] of the memory bus.

h. *Said second-endian processor executes a second program that defines structure data which includes data that is smaller than the basic word length, the data being defined in an order within the basic word length, and the order being in reverse to an order in the first program*. Column 9 lines 22-25 shows that when a processor in bit-endian mode, DSP 400, writes a 16 bit value to location 2 of memory word 410, it will overwrite 0xBBAA, corresponding to lines [15:0] of the memory bus. To ensure accesses to data objects smaller than the size of the data bus are properly aligned, as discussed at column 9 lines 25-33, memory controller circuitry 706 as discussed at column 10 lines 59 through column 11 line 4 inverts lower order address bits when accesses smaller than a word are made into a memory region storing data in corresponding to a different endianness than the requesting resource.

i. *And said first-endian processor reads or writes the structure data to communicate with said second-endian processor, and said second-endian processor reads or writes the structure data to communicate with said first-endian processor*. Column 8 lines 63-65 shows that figure 4 is an illustration of

two processors of different endianness accessing the same memory location 410. By accessing the same memory location the two processors are communicating using reads and/or writes to the memory location.

14. Lasserre teaches, at column 10 line 55 through column 11 line 4, that the bits of the address are inverted by address adjustment circuitry 706 according to the data size signals 708, but does not expressly disclose which bits are inverted for different data access sizes.

15. With respect to claim 9, Sartorius teaches how bits of an address are adjusted to account for accesses to memory locations containing data stored in a different endian format, See column 1 line 58 through column 2 line 25. The Examiner points out that the example discussed in Sartorius is a system using a 64 bit bus, therefore the three least significant bits of the address must be considered, as there are 8 positions that a 1 byte element may be aligned in a 64 bit bus. The Examiner notes that the example given in figure 4 of Lasserre uses a 32 bit bus, see column 9 lines 4-5. In a system using a 32 bit bus, only the two least significant bits would need to be adjusted, as there are only 4 positions that a 1 byte element may be aligned.

j. *(i) to invert values of two least significant bits of an address outputted from said second-endian processor and output an address including the inverted values to said memory when said second-endian processor performs a memory access for 8-bit data*. The table shown in figure 1 shows that when a request is made for a 1 byte (8 bit) element, the three least significant bits of the address are XORed with 111, which inverts the two least significant bits of the address.

k. *(ii) to invert a value of a second least significant bit of an address outputted from said second-endian processor and output an address including the inverted value to said memory when said second-endian processor performs a memory access for 16-bit data*. The table shown in figure 1 shows that when a request is made for a 2 byte (16 bit) element, the three least significant bits of the address are XORed with 110, which inverts the second least significant bit but does not invert the least significant bit.

l. *And (iii) to output an address from said second-endian processor to the memory without address conversion when said second-endian processor performs a memory access for data having the width of the first data bus*. The table shown in figure 1 shows that when a request is made for an element having the width of the data bus, an 8-byte element, no modification to the address is made.

16. Lasserre and Sartorius are analogous art because they are from the same field of endeavor, systems making access to data stored in memory in differing endian formats.

17. At the time of the invention, it would have been obvious to one of ordinary skill in the art for the address adjustment circuitry 706 of Lasserre to invert the least significant bits of the memory address as shown by Sartorius in figure 1.

18. The suggestion for doing so comes from Lasserre column 10 line 63 through column 11 line 9, which states that the physical address bits are inverted according to data size signals, and that the inversion may be performed by XOR gates.

19. Therefore, it would have been obvious to combine Sartorius with Lasserre for the benefit of properly accessing memory elements of differing endianism to obtain the invention as specified in **claims 9**.

20. **Claim 10** is taught by Lasserre as:

m. *The data sharing apparatus according to Claim 9, further comprising a transfer unit operable to control data transfer by direct memory access*. Resources 540 of figure 5, as discussed at column 9 lines 34-41, include DMA engine 106. Column 10 lines 3-4 shows that resource 700 of figure 7 is representative of one or more or resources 540 or 550, and therefore is representative of DMA 106.

n. *Wherein, in the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred, the transfer unit reverses an order of said data within a basic word length, for the source and the destination*. Column 10 line 59 through column 11 line 4 shows that memory controller circuitry 706, responsive to size signals 708, inverts the least significant address bits to reverse the address ascension in order to agree with the endianism of the selected memory region.

21. **Claim 11** is taught by Lasserre as:

o. *The data sharing apparatus according to Claim 10, wherein the transfer unit includes a conversion unit operable to convert at least one lower bit of an*

*address of either the source or the destination so as to indicate a reversed position of the data in the data bus*. Column 10 lines 44-45 shows that resource 700 is representative of one or more resources 540 or 550, which includes the DMA engine. Column 10 line 59 through column 11 line 4 shows that memory controller circuitry 706 inverts the least significant address bits to reverse the address ascension in order to agree with the endianism of the selected memory region.

p. *And output the converted address to the memory*. Figure 7 shows adjusted physical address 716 being output from address adjust circuitry 706.

q. *In the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred*. Column 9 lines 18-33 show that only data objects smaller than the size of the data portion of the external memory interface require adjusted offsets on the data bus. Column 10 lines 52-62 show that memory controller circuitry 706 is responsive to size signals 708, which define the byte size of each memory transaction request, and endianism attribute signal 710.

22. **Claim 16** is taught by Lasserre as:

r. *A data sharing apparatus comprising: a data bus having a data width*. Column 8 lines 63-65 show DSP 400 sharing a memory location 410 with a CPU 402, with the DSP 400 and CPU 402 having different endianness. Column 9 4-17 shows that the data bus between the processors and memory is 32 bits.

s. *A memory*. Figure 4 shows a memory storing memory location 410.

t. *A first-endian processor logically connected to said memory in a first-endian byte order via said data bus*. CPU 402.

u. *A second-endian processor logically connected to said memory in the first-endian byte order via said data bus*. DSP 400. Figure 4, as discussed in column 9 lines 12-17, shows that each of the processors are connected to the data bus such that inputs [7:0] of the two processors and the memory are connected to the same lines of the data bus.

v. *And an address conversion unit operable to invert selected address bits and output the adjusted address*. Column 10 line 59 through column 11 line 4 shows that memory controller circuitry 706 inverts the least significant address bits to reverse the address ascension in order to agree with the endianism of the selected memory region. Figure 7 shows adjusted physical address 716 is output by address adjust circuitry 706.

w. *A cache memory logically connected to the data bus in a second-endian byte order*. Figure 2B shows L2 Cache 114 connected to L2 traffic control 110. Column 3 lines 52-54 shows that the DSP as shown in figure 2 is connected to the traffic controller via L2 interface 210, which includes TLB 212. Column 8 lines 42-50 shows that each TLB entry contains information about the endianism of the memory address region represented by the TLB entry. Accordingly, the data stored in the L2 memory, shown at column 3 lines 10-14 to include cache 114, can be stored in either little or big endian format. When data in the second-

endian byte order is being accessed, cache 114 is logically connected to traffic control 110 in a second-endian byte order.

x. *Wherein said memory stores structure data to be accessed by said first-endian processor and said second-endian processor*. Column 9 lines 22-25 shows that a 16 bit value can be written to location 2 of 32 bit memory word 410 of figure 4.

y. *Said first-endian processor executes a first program that defines the structure data*. As a processor can only access data under the control of a program, it is inherent that the 16 bit value, smaller than the 32 bit word size, is accessed by a program executing on the processor. Column 9 lines 22-25 show that the memory access can be performed by either the big endian or little endian processor.

z. *And said second-endian processor executes a second program that defines structure data which includes data that is smaller than the basic word length, said data being defined in an order within the basic word length, and said order being in reverse to an order in the first program*. Column 9 lines 22-25 show that the memory access can be performed by either the big endian or little endian processor.

aa. *And said first-endian processor reads or writes the structure data to communicate with said second-endian processor, and said second endian processor reads or writes the structure data to communicate with said first-endian processor*. Column 8 lines 63-65 shows that figure 4 is an illustration of

two processors of different endianness accessing the same memory location 410. By accessing the same memory location the two processors are communicating using reads and/or writes to the memory location.

23. Lasserre teaches, at column 10 line 55 through column 11 line 4, that the bits of the address are inverted by address adjustment circuitry 706 according to the data size signals 708, but does not expressly disclose which bits are inverted for different data access sizes.

24. With respect to claim 16, Sartorius teaches how bits of an address are adjusted to account for accesses to memory locations containing data stored in a different endian format, See column 1 line 58 through column 2 line 25. The Examiner points out that the example discussed in Sartorius is a system using a 64 bit bus, therefore the three least significant bits of the address must be considered, as there are 8 positions that a 1 byte element may be aligned in a 64 bit bus. The Examiner notes that the example given in figure 4 of Lasserre uses a 32 bit bus, see column 9 lines 4-5. In a system using a 32 bit bus, only the two least significant bits would need to be adjusted, as there are only 4 positions that a 1 byte element may be aligned.

bb. *(i) to invert values of two least significant bits of an address outputted from said second- endian processor and output an address including the inverted values to said memory when said second-endian processor performs a memory access for 8-bit data*. The table shown in figure 1 shows that when a request is made for a 1 byte (8 bit) element, the three least significant bits of the address are XORed with 111, which inverts the two least significant bits of the address.

cc. *(ii) to invert a value of a second least significant bit of an address outputted from said second- endian processor and output an address including the inverted value to said memory when said second-endian processor performs a memory access for 16-bit data*. The table shown in figure 1 shows that when a request is made for a 2 byte (16 bit) element, the three least significant bits of the address are XORed with 110, which inverts the second least significant bit but does not invert the least significant bit.

dd. *And (iii) to output an address from said second-endian processor to the memory without address conversion when said second-endian processor performs a memory access for data having the width of the first data bus*. The table shown in figure 1 shows that when a request is made for an element having the width of the data bus, an 8-byte element, no modification to the address is made.

25. Lasserre and Sartorius are analogous art because they are from the same field of endeavor, systems making access to data stored in memory in differing endian formats.

26. At the time of the invention, it would have been obvious to one of ordinary skill in the art for the address adjustment circuitry 706 of Lasserre to invert the least significant bits of the memory address as shown by Sartorius in figure 1.

27. The suggestion for doing so comes from Lasserre column 10 line 63 through column 11 line 9, which states that the physical address bits are inverted according to data size signals, and that the inversion may be performed by XOR gates.

28. Therefore, it would have been obvious to combine Sartorius with Lasserre for the benefit of properly accessing memory elements of differing endianism to obtain the invention as specified in **claims 16**.

29. **Claim 17** is taught by Lasserre as:

ee. *The data sharing apparatus according to Claim 16, further comprising a transfer unit operable to control data transfer by direct memory access*. Figure 5 shows resources 540, which include a DMA engine. Column 10 lines 28-41 discuss the steps taken when an endianism mismatch is detected.

ff. *Wherein, in the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred, the transfer unit reverses an order of said data within a basic word length, for the source and the destination*. As shown in column 10 lines 34-41, when an endianism mismatch occurs, the abort handler invokes a software routine that converts the data to an alternative endian format.

30. **Claim 18** is taught by Lasserre as:

gg. *The data sharing apparatus according to Claim 17, wherein the transfer unit includes a conversion unit operable to convert at least one lower bit of an address of either the source or the destination so as to indicate a reversed position of the data in the data bus*. Column 10 lines 44-45 shows that resource 700 is representative of one or more resources 540 or 550, which includes the

DMA engine. Column 10 line 59 through column 11 line 4 shows that memory controller circuitry 706 inverts the least significant address bits to reverse the address ascension in order to agree with the endianism of the selected memory region.

hh. *And output the converted address to the memory*. Figure 7 shows adjusted physical address 716 being output from address adjust circuitry 706.

ii. *In the case where a source and a destination require data of different endianness and data with a smaller width than the width of the data bus is to be transferred*. Column 9 lines 18-33 show that only data objects smaller than the size of the data portion of the external memory interface require adjusted offsets on the data bus. Column 10 lines 52-62 show that memory controller circuitry 706 is responsive to size signals 708, which define the byte size of each memory transaction request, and endianism attribute signal 710.

31. **Claim 19** is taught by Lasserre as:

jj. *A method of sharing data in a data processing apparatus which includes a first-endian type processor and a second-endian type processor, and a memory to which both processors are connected via a data bus in a first-endian byte order*. Column 8 lines 63-65 show DSP 400 sharing a memory location 410 with a CPU 402, with the DSP 400 and CPU 402 having different endianness. Figure 4, as discussed in column 9 lines 12-17, shows that each of the processors are

connected to the data bus such that inputs [7:0] of the two processors and the memory are connected to the same lines of the data bus.

kk. *The method comprising: causing the first processor to execute a program that defines structure data, causing the second processor to execute a program that defines structure data which includes data that is smaller than a basic word length, said structure data being shared in the memory, said data being defined in an order within the basic word length, and said order being in reverse to an order in a definition of said structure data for the first-endian type processor*. Column 9 lines 18-25 shows that the processors of different endianness can access data objects smaller than a word, and that because the different processors have different endianness, the order of the byte addresses is reversed, as shown in figure 4. As the processors are accessing the shared memory location, it is inherent that they are each executing a program that causes them to do so, as processors do not access memory if they are not executing a program.

ll. *Causing the first endian processor to read or write the structure data to communicate with the second-endian processor, and causing the second endian processor to read or write the structure data to communicate with the first-endian processor*. Column 8 lines 63-65 shows that figure 4 is an illustration of two processors of different endianness accessing the same memory location 410. By accessing the same memory location the two processors are communicating using reads and/or writes to the memory location.

32. Lasserre teaches, at column 10 line 55 through column 11 line 4, that the bits of the address are inverted by address adjustment circuitry 706 according to the data size signals 708, but does not expressly disclose which bits are inverted for different data access sizes.

33. **With respect to claim 19**, Sartorius teaches how bits of an address are adjusted to account for accesses to memory locations containing data stored in a different endian format, See column 1 line 58 through column 2 line 25. The Examiner points out that the example discussed in Sartorius is a system using a 64 bit bus, therefore the three least significant bits of the address must be considered, as there are 8 positions that a 1 byte element may be aligned in a 64 bit bus. The Examiner notes that the example given in figure 4 of Lasserre uses a 32 bit bus, see column 9 lines 4-5. In a system using a 32 bit bus, only the two least significant bits would need to be adjusted, as there are only 4 positions that a 1 byte element may be aligned.

mm. *(i) inverting values of two least significant bits of an address outputted from the second-endian processor and outputting an address including the inverted values to said memory when the second-endian processor performs a memory access for 8-bit data*. The table shown in figure 1 shows that when a request is made for a 1 byte (8 bit) element, the three least significant bits of the address are XORed with 111, which inverts the two least significant bits of the address.

nn. *(ii) inverting a value of a second least significant bit of an address outputted from the second-endian processor and outputting an address including*

*the inverted value to said memory when the second-endian processor performs a memory access for 16-bit data*. The table shown in figure 1 shows that when a request is made for a 2 byte (16 bit) element, the three least significant bits of the address are XORed with 110, which inverts the second least significant bit but does not invert the least significant bit.

oo. *And (iii) outputting an address from the second-endian processor to the memory without address conversion when the second-endian processor performs a memory access for data having the width of the first data bus*. The table shown in figure 1 shows that when a request is made for an element having the width of the data bus, an 8-byte element, no modification to the address is made.

34. Lasserre and Sartorius are analogous art because they are from the same field of endeavor, systems making access to data stored in memory in differing endian formats.

35. At the time of the invention, it would have been obvious to one of ordinary skill in the art for the address adjustment circuitry 706 of Lasserre to invert the least significant bits of the memory address as shown by Sartorius in figure 1.

36. The suggestion for doing so comes from Lasserre column 10 line 63 through column 11 line 9, which states that the physical address bits are inverted according to data size signals, and that the inversion may be performed by XOR gates.

37. Therefore, it would have been obvious to combine Sartorius with Lasserre for the benefit of properly accessing memory elements of differing endianism to obtain the invention as specified in **claims 19**.

38. **Claims 24 and 26** are taught by Lasserre as:

pp. *Wherein the first-endian type is big-endian and the second-endian type is little-endian*. Column 10 lines 42-63 shows that each resource 700, which includes resources 540 or 550, which is shown at column 9 lines 40-46 to include DMA engine 106, coprocessors 108, and processors 102 and 104, contains an endianism-ID circuitry 712 and memory controller 706. The addresses are adjusted when the endianism of resource 700, indicated by endianism-ID circuitry 712, does not match the endianism of the memory region being accessed, indicated by endianism attribute signal 710. Accordingly, when the processor is little-endian, the second-endian type, such as CPU 402 of figure 4, and performs a sub-word memory access to a region of memory that stored data in a big-endian format as indicated by endianism attribute signal 710, the processing recited in claims 21, 24, and 26 is performed.

39. **Claim 25 and 27** are taught by Lasserre as:

qq. *The processor according to claim 20, wherein the first-endian type is little-endian and the second-endian type is big-endian*. Column 10 lines 42-63 shows that each resource 700, which includes resources 540 or 550, which is shown at

column 9 lines 40-46 to include DMA engine 106, coprocessors 108, and processors 102 and 104, contains an endianism-ID circuitry 712 and memory controller 706. The addresses are adjusted when the endianism of resource 700, indicated by endianism-ID circuitry 712, does not match the endianism of the memory region being accessed, indicated by endianism attribute signal 710. Accordingly, when the processor is big-endian, the second-endian type, such as DSP 400 of figure 4, and performs a sub-word memory access to a region of memory that stored data in a little-endian format as indicated by endianism attribute signal 710, the processing recited in claims 21, 24, and 26 is performed.

40. **Claim 28** is taught by Lasserre as:

rr. *A data sharing apparatus comprising: a first-endian processor operable to execute a first program in which a first structure data is defined*. MPU processor 102.

ss. *A first-endian type memory operable to store shared data*. Memory subsystem 112, column 3 lines 10-15 show that MPU 102 and DSP 104 share memory subsystem 112. Column 5 lines 1-9 shows that the MMU provides a shared bit and endianism information. Column 8 lines 42-55 shows that the TLB entries contain an endianness attribute bit, as some sections of the memory may be big endian and some sections may be little endian. Accordingly, sections storing data in the endian format used by MPU 102 provide first endian type memory.

tt. *A first address bus logically connected to said first-endian processor and said first-endian type memory*. Fig 2B shows MPU 102 connected to traffic control 110 over an address bus, shown as a single-directional arrow between items 102 and 110.

uu. *A first data bus logically connected to said first-endian processor and said first-endian type memory*. Fig 2B shows MPU 102 connected to traffic control 110 over a data bus, shown as a bi-directional arrow between items 102 and 110.

vv. *A second-endian processor operable to execute a second program in which a second structure data is defined and to communicate with said first-endian processor via the shared data stored in said first-endian type memory*. DSP processor 104 of figure 1. Column 8 line 63 through column 9 show that DSPs and processors having different endianness can access data in shared regions of memory.

ww. *A second address bus which is logically connected to said second-endian processor*. Fig 2A shows DSP 104 connected to traffic control 110 over an address bus, shown as a single-directional arrow between items 104 and 110.

xx. *A second data bus logically connected to said second-endian processor, said second data bus being logically connected to the first data bus in a first-endian order*. Fig 2A shows DSP 104 connected to traffic control 110 over a data bus, shown as a bi-directional arrow between items 104 and 110.

yy. *And an address conversion unit, logically connected to said first address bus and said second address bus*. Column 10 line 59 through column 11 line 4 shows that each memory initiator resource can contain memory controller circuitry 706.

zz. *Wherein the shared data is defined as the first structure data in said first-endian processor and is defined as the second structure data in said second-endian processor*. Column 8 line 63 through column 9 line 3 shows that DSPs and processors having different endianness can access data in shared regions of memory. Column 9 lines 4-6 shows that the data accessed may be a 32 bit word.

aaa. *The first structure data and the second structure data include data that is smaller than a basic word length, the data being defined in an order within the basic word length*. Column 9 lines 18-25 shows the different endian processors accessing a 8 bit and a 16 bit object.

bbb. *The order in a definition of the first structure data being in reverse to an order in a definition of the second structure data*. Column 8 lines 48-55 shows that a little endian processor views data objects with ascending addresses at more significant places on the data bus, and a processor is big endian if data objects with ascending addresses appear at less significant places on the data bus.

ccc. *And said first-endian processor reads or writes the shared data to communicate with said second-endian processor and said second-endian*

*processor reads or writes the shared data to communicate with said first-endian processor*. Column 8 lines 63-65 shows that figure 4 is an illustration of two processors of different endianness accessing the same memory location 410. By accessing the same memory location the two processors are communicating using reads and/or writes to the memory location.

41. Lasserre teaches, at column 10 line 55 through column 11 line 4, that the bits of the address are inverted by address adjustment circuitry 706 according to the data size signals 708, but does not expressly disclose which bits are inverted for different data access sizes.

42. **With respect to claim 28**, Sartorius teaches how bits of an address are adjusted to account for accesses to memory locations containing data stored in a different endian format, See column 1 line 58 through column 2 line 25. The Examiner points out that the example discussed in Sartorius is a system using a 64 bit bus, therefore the three least significant bits of the address must be considered, as there are 8 positions that a 1 byte element may be aligned in a 64 bit bus. The Examiner notes that the example given in figure 4 of Lasserre uses a 32 bit bus, see column 9 lines 4-5. In a system using a 32 bit bus, only the two least significant bits would need to be adjusted, as there are only 4 positions that a 1 byte element may be aligned.

ddd. *(i) to invert values of two least significant bits of an address in said second address bus and output an address including the inverted values to said first address bus when said second-endian processor performs a memory access for 8-bit data*. The table shown in figure 1 shows that when a request is made for a

1 byte (8 bit) element, the three least significant bits of the address are XORed with 111, which inverts the two least significant bits of the address.

eee. *(ii) to invert a value of a second least significant bit of an address in said second address bus and output an address including the inverted value to said first address bus when said second-endian processor performs a memory access for 16-bit data*. The table shown in figure 1 shows that when a request is made for a 2 byte (16 bit) element, the three least significant bits of the address are XORed with 110, which inverts the second least significant bit but does not invert the least significant bit.

fff. *And (iii) to output an address from said second address bus to said first address bus without address conversion when said second-endian processor performs a memory access for data having the width of the first data bus*. The table shown in figure 1 shows that when a request is made for an element having the width of the data bus, an 8-byte element, no modification to the address is made.

43. Lasserre and Sartorius are analogous art because they are from the same field of endeavor, systems making access to data stored in memory in differing endian formats.

44. At the time of the invention, it would have been obvious to one of ordinary skill in the art for the address adjustment circuitry 706 of Lasserre to invert the least significant bits of the memory address as shown by Sartorius in figure 1.

45. The suggestion for doing so comes from Lasserre column 10 line 63 through column 11 line 9, which states that the physical address bits are inverted according to data size signals, and that the inversion may be performed by XOR gates.

46. Therefore, it would have been obvious to combine Sartorius with Lasserre for the benefit of properly accessing memory elements of differing endianism to obtain the invention as specified in **claim 28**.

### ***Response to Arguments***

47. Applicant's arguments submitted 1/28/2008 have been carefully and fully considered, but are not found persuasive.

48. **First point of Argument**

49. In the sixth paragraph beginning on page 11 of the Arguments submitted 1/28/2008, with respect to the claims 9, 16, 19, and 28, Applicant argues:

> ggg. "*According to the above-mentioned claim limitation (A), the sharing of data having the width of the data bus between said processor and the processor of a different endianness, via the memory, can be implemented with an extremely simple structure (i.e., simply with a bus connection as recited in feature (A), rather than through a time consuming software conversion process)*."

50. The Examiner respectfully disagrees. Figure 4 of Lasserre shows that Data lines [7:0] of both the DSP 400 and CPU 402 are connected to the same data, [M7:0], despite the fact that lines [7:0] of the CPU correspond to byte 0 of a little endian processor and lines [7:0] of the DSP correspond to byte 3 of a big endian processor, Accordingly, they

are both connected in a first-endian byte order. The Examiner further notes that this is the same connections shown in figures 7 and 16 of the instant application.

51. **Second point of Argument**

52. In the sixth through eleventh paragraph beginning on page 14, Applicant argues differences between the embodiment disclosed in figure 6 of Lasserre. The Examiner respectfully refers Applicant to the embodiment disclosed in figure 7 of Lasserre, relied upon in the rejection, which teaches the use of hardware conversion of address bits when a memory access is made to a region having an endianism mismatch.

**53. Third point of Argument**

54. In the second paragraph beginning on page 15, with respect to Lasserre's teaching of features (i), (ii), and (iii), the Examiner respectfully submits that Applicant's arguments are moot as Lasserre was not relied upon for such a teaching.

55. **Fourth point of Argument**

56. In the third paragraph beginning on page 15, with respect to Lasserre's teaching of concern for data width, Applicant argues:

> hhh. "*With regard to "data positioning", (i.e., the claimed features of the logical connection (A) to the bus and (C) defining of structure data in reverse order in claims 9, 16, 19, and 28), Lasserre performs the same process as in the case in TABLE 1. Since the judgment for endianism mismatch in FIG. 6 in Lasserre is not concerned with data width, the above process (FIG. 6; col. 10, lines 34 to 41) is carried out without distinguishing between memory access for data having the same width as the data bus and memory access for data having a smaller width*

*than the data bus. In other words, the process details are the same for the case where the data width is the same as the bus and the case where data width is smaller. Therefore, as previously mentioned, in Lasserre, the aborting of the memory access, the changing of endianism through the rewriting of the memory region, and the re- accessing of the memory occur when a processor of different endianness performs memory access for data having a smaller width than the data bus*."

57. The Examiner respectfully disagrees. Column 10 lines 52-54 states: "Processor core 702 also provides size signals 708 to define the byte size of each memory transaction request." Column 11 lines 1-2 states: "the physical address bits will be adjusted by inverting selected bits according to data size signals 708 in order to reverse the address ascension order to agree with the endianism of the selected memory region. Again, the Examiner respectfully points out that it appears Applicant is arguing characteristics of the embodiment discussed in figure 6, while the Examiner is relying on the embodiment disclosed in figure 7.

58. **Fifth point of Argument**

59. In the sixth and seventh paragraphs beginning on page 16 and continuing on page 17, with respect to Lasserre's teaching of processing for "data positioning," Applicant argues:

iii. "*The Examiner argues that this point is disclosed in the structure data in FIG. 4 of Lasserre. However, Applicants believe that the Examiner's interpretation is incorrect because, if it were to be assumed that FIG. 4 in*

*Lasserre disclosed structure data defined in reverse order, there would be a contradiction with the descriptions of the data positioning (col. 9, lines 30 to 33) and the memory region endian conversion (FIG. 6; col. 10, lines 34 to 41) in the Specification of Lasserre. In other words, when structure data that is defined in reverse order is applied in Lasserre, "data positioning" is applied twice over and memory access of data in the correct byte order will not be possible*.

jjj. *Therefore, Applicants assert that FIG. 4 in Lasserre illustrates register data, and not structure data. In other words, FIG. 4 of Lasserre is properly interpreted as merely describing that in order to correctly share data, data should be shared in this manner in the register 404 of the big-endian processor 400, and the register 406 in the little-endian processor 402*."

60. The Examiner respectfully disagrees. The Examiner wishes to point out that items 404 and 406 are not identified in the disclosure of Lasserre as being registers, Column 9 lines 12-17 shows that items 404 and 406 are byte lanes. The Examiner also wishes to draw applicant's attention to column 8 line 63 through column 9 line 3, which shows that DSP 400 and CPU 402 are accessing a same memory location 401, and that a fundamental requirement is that external memory is connected to the processor so that accesses to 32-bit objects yield the same results in both big and little endian modes. The Examiner further would like to draw Applicant's attention to column 8 lines 56-62, which show that any shifting required to access objects smaller than 32 bits occurs inside the processor. The Examiner respectfully notes that if the structure data smaller than the data bus, i.e. 16 and 8 bit objects, were not defined in reverse order on

the data bus, there would be no shifting required, as the data received on data lines D[7:0] would be already be in the proper location.

***Conclusion***

61. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JARED I. RUTZ whose telephone number is (571)272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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